6. The array of photodiodes of claim 1, wherein said conductive layer comprises a polysilicon layer.

7. The array of photodiodes of claim 1, further comprising a silicon nitride layer over said conductive layer.

8. The array of photodiodes of claim 1, wherein said semiconductive region of first conductivity type comprises a semiconductor substrate made of single-crystal silicon, said at least one insulating layer comprises a silicon oxide layer and said conductive layer comprises a polysilicon layer.

9. The array of photodiodes of claim 8, further comprising a silicon nitride layer over said conductive layer.

10. The array of photodiodes of claim 9, wherein said single-crystal silicon layer and said polysilicon layer have a high refraction coefficient on the order of 4, while said silicon oxide layer and silicon nitride layer have a lower coefficient, on the order of 1.5.

11. The array of photodiodes of claim 1, wherein said conductive layer is connected to said semiconductive region of a first conductivity type at a heavily doped P-type region 8 thereof.

12. A photodiode comprising:

a semiconductor substrate of first conductivity type;

a semiconductive region of second conductivity type and formed in said semiconductor substrate;

a multilayer interference filter disposed over said semiconductive region and including;

at least one insulating layer of predetermined thickness, and

a conductive layer disposed over said at least one insulating layer,

wherein said conductive layer includes a conductive portion that electrically connects said conductive layer to said semiconductor substrate of first conductivity type.

13. The photodiode of claim 12, wherein said semiconductor substrate comprises a single-crystal silicon.

14. The photodiode of claim 13, wherein said at least one said insulating layer comprises a silicon oxide layer.

15. The photodiode of claim 14, wherein said conductive layer comprises a polysilicon layer.

16. The photodiode of claim 15, further comprising a silicon nitride layer over said conductive layer.

17. A photodiode comprising:

a semiconductor substrate of first conductivity type;

a semiconductive region of second conductivity type and formed in said semiconductor substrate;

a multilayer interference filter disposed over said semiconductive region and including;

at least one insulating layer of predetermined thickness, and

a conductive layer disposed over said at least one insulating layer,

means defining a conductive portion that electrically connects said conductive layer to said semiconductor substrate of first conductivity type.

18. The photodiode of claim 17, further including means defining a heavily doped region of said semiconductor substrate to which said conductive portion couples.

19. A photodiode circuit comprising a photodiode, a precharged transistor, said photodiode having its cathode coupled to the source of the precharge transistor, the drain of said precharge transistor being connected to a reference voltage and the gate of said precharge transistor connected to a roll line meant to select all of the transistors of the same row, and an

amplifier transistor having its gate connected to the cathode of said photodiode and its source connected to a column line.

20. A method for forming oxide layers over three groups of cathode regions, comprising the steps of:

depositing a first silicon oxide layer over a substrate and etching the layer to maintain it in place above a first region;

depositing and etching a second silicon oxide layer to leave it in place above first and second regions; and

depositing a third silicon oxide layer over all three said regions.

21. The method of claim 20, further depositing a polysilicon layer over the third silicon oxide layer.

22. The method of claim 20, wherein the first silicon oxide layer has a thickness on the order of 40 nm, the second silicon oxide layer has a thickness on the order of 40 nm and the third silicon oxide layer has a thickness on the order of 150 nm.

23. A method of forming a pixel of an image sensor comprising the steps of:

providing a silicon substrate;

defining a precharge transistor and a diode in the silicon substrate;

forming a drain region of the transistor and a source region of the transistor in the substrate;

the source region extending to form the cathode region of the diode, the anode of which corresponds to the substrate;

forming an insulated gate between the drain and source of the transistor;

providing an insulating layer over the source region; and

providing a conductive layer over the insulating layer.

24. The method of claim 23, wherein the substrate is a P-type single-crystal silicon substrate, the drain region is of N-type and the source region is of N-type.

25. The method of claim 23, wherein said cathode region forms one piece with a metallization connected to the gate of the transistor.

26. The method of claim 23, further including forming a conductive portion that interconnects the conductive layer to the substrate.

27. A photodiode comprising:

a semiconductor substrate of first conductivity type;

a semiconductive region of second conductivity type and formed in said semiconductor substrate;

a multilayer interference filter disposed over said semiconductive region and including;

at least one insulating layer of predetermined thickness, and

a conductive layer disposed over said at least one insulating layer,

said semiconductor substrate defining a well formed in a base substrate of second conductivity type, said conductive layer being connected to said base substrate.

REMARKS

In response to the Office Action mailed June 26, 2000, Applicant respectfully requests reconsideration. To further the prosecution of this case, arguments are submitted herewith, and Applicant has furthermore added several additional claims to this application.

In the Office Action the Examiner has rejected claims 1-3 under 35 U.S.C. 103 as unpatentable over Koike et al. The Examiner has made reference to Fig. 2 of that patent along with column 4 at lines 4-7 and 46-52. The Examiner has furthermore taken the position that it would be obvious to have the substrate at ground and electrodes 13 either connected to the substrate or via a fixed potential.

The Examiner has also rejected claim 1 under 35 U.S.C. §102 relying upon the patent to Nagasaki et al. The Examiner refers to Fig. 1 of that patent and layers 4 and 9.

Applicant respectfully disagrees with this rejection. Koike discloses an imaging device comprising cells respectively allotted to red, blue or green colors. The regions corresponding to the different colors are covered with an optical filter 101 consisting of a striped color filter